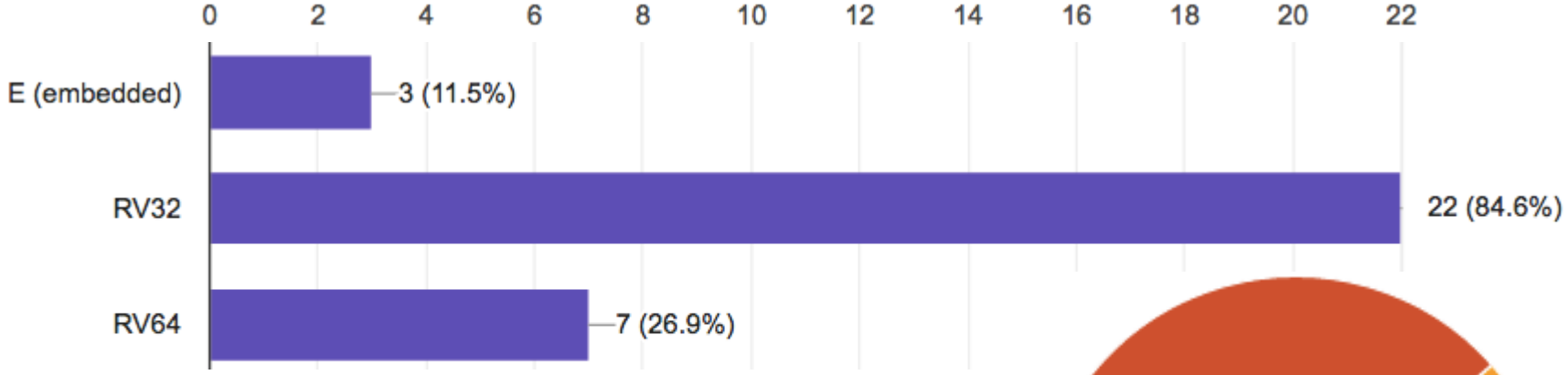
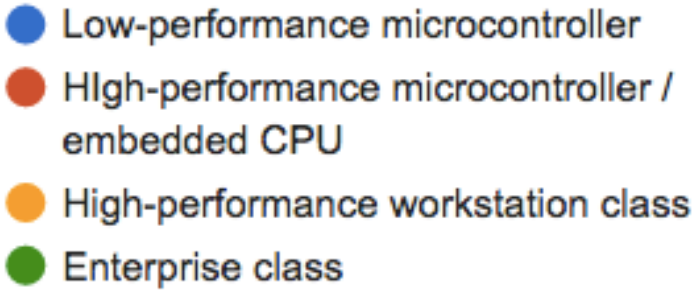
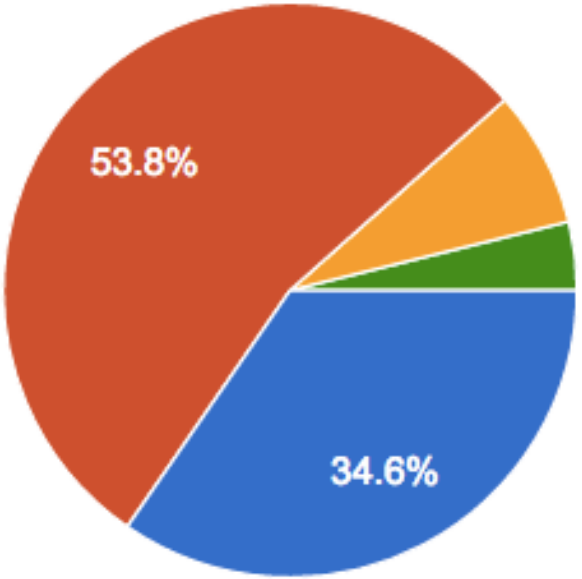
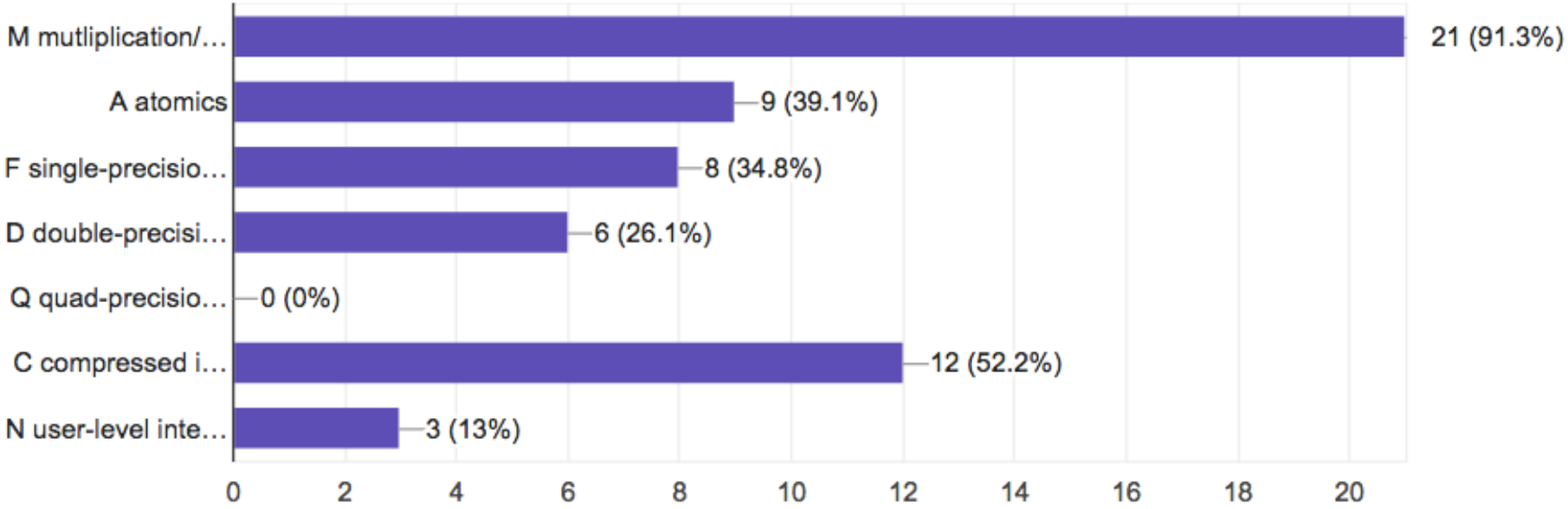
2017 Survey: 26 RISC- V CPU Designs





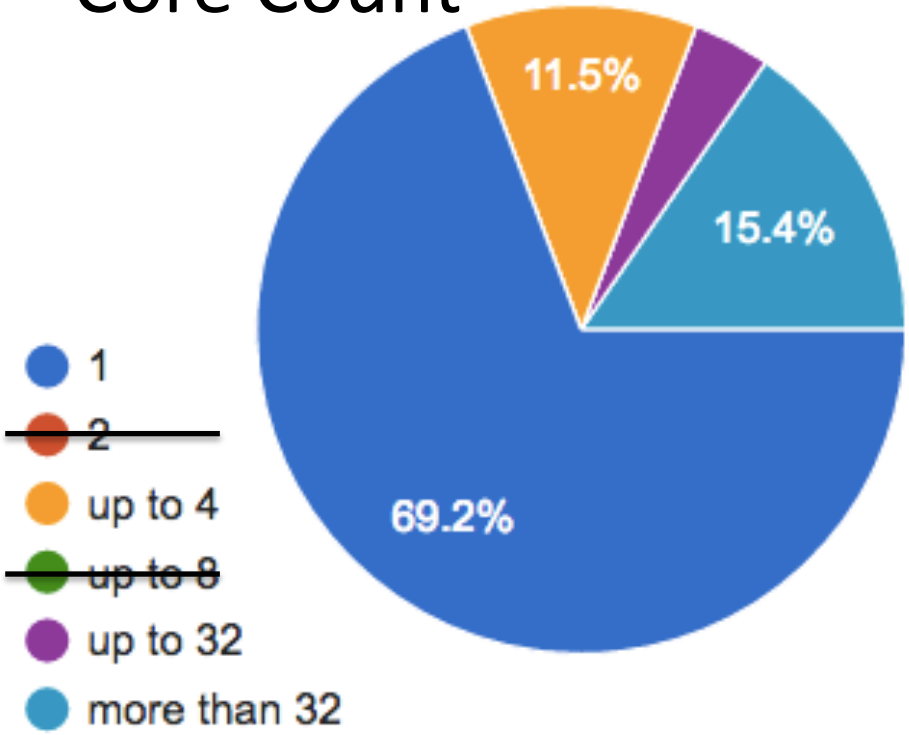


2017 Survey: Standard Extensions

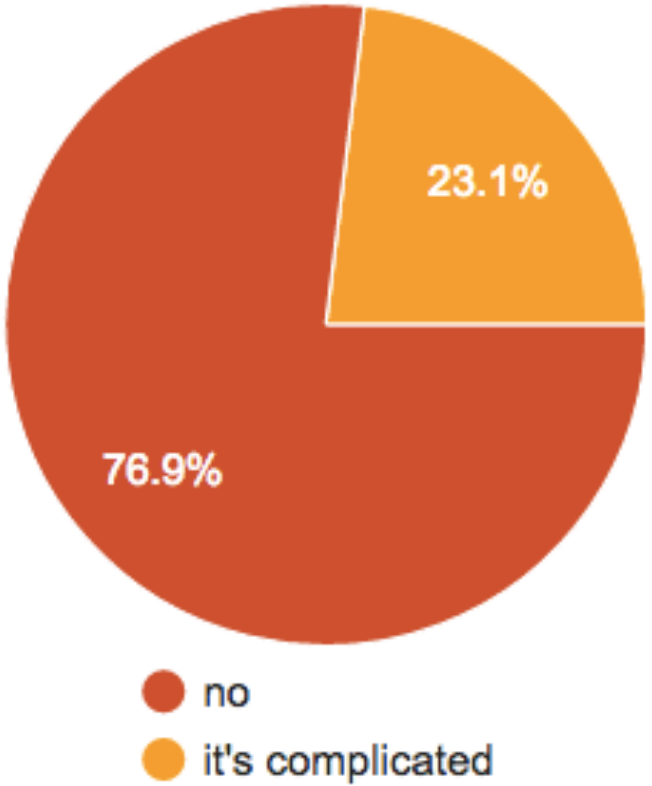


2017 Survey: Multicore

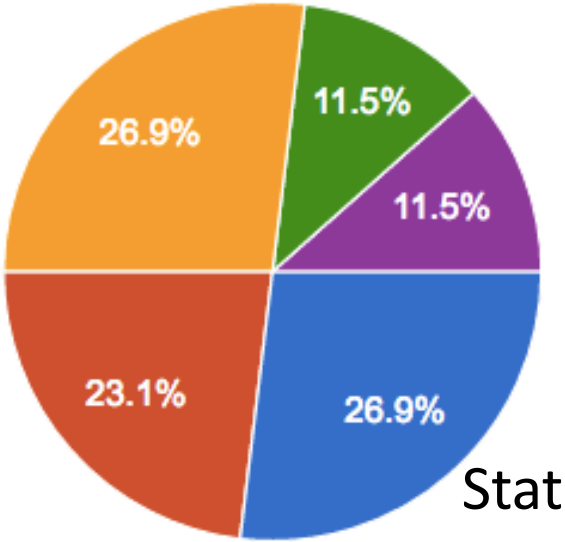
Core Count



big.LITTLE

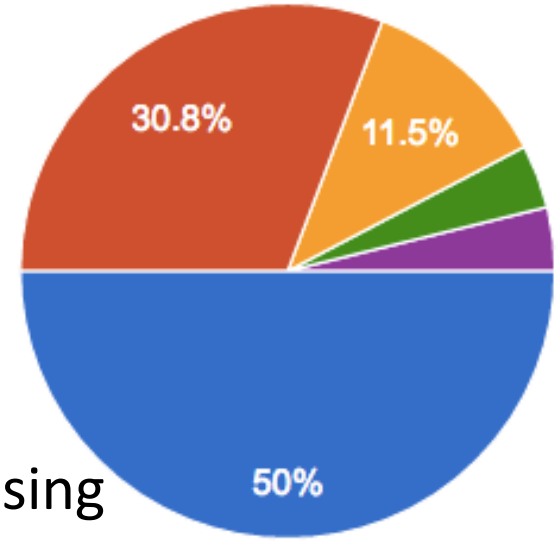


Survey: Availability



Status

- In development
- Works in research lab
- In a select few customer labs
- In many customer labs
- Fully shipping



Licensing

- open source
- for fee under license
- privately held / may be available at some point
- privately held / unavailable / please don't ask us
- it's complicated

RISC-V CPU Survey Respondents

Rocket	github.com/freechipsproject/
Freedom Everywhere	SiFive.com
Mythic IPU	mythic-ai.com
riscV	n/a
PulpTR	ankasys.com
proc_rv32ec_p2	astc-design.com
proc_rv32ic_p5	astc-design.com
KCP53000	kestrelcomputer.github.io/kestrel
RV12	roalogic.com
PicoRV32	github.com/cliffordwolf/picorv32
Klessydra processing core	en.uniroma1.it
BOOM	ucb-bar.github.io/riscv-boom
PULP	github.com/pulp-platform

RV01	n/a
IntenCore	intensivate.com
YARVI	github.com/tommythorn/yarvi
RISCVBusiness	purduesoceet.github.io
GRVI Phalanx	fpga.org/gray-research-llc
SCR1	syntacore.com
SCR2	syntacore.com
SCR3	syntacore.com
SCR4	syntacore.com
SCR5	syntacore.com
Celerity	n/a
riscv-lanzones	github.com/e19293001/riscv-lanzones
ORCA	github.com/vectorblox/orca